IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A processor comprising:

a plurality of hardware functional units within the processor, the hardware functional units including a first hardware functional unit and a second hardware functional unit, the first hardware functional unit to receive instructions, to determine whether ones of the instructions are associated with a virus, and to transmit the ones of the instructions not associated with the virus to the second hardware functional unit; and

wherein the first hardware functional unit is a hardware functional unit dedicated to functions associated to virus detection.

2. (Currently Amended) The processor of claim 1, wherein the first hardware functional unit is a virus detection unit, and wherein the second hardware functional unit is a fetch and decode unit.

3. (Currently Amended) The processor of claim 1, wherein the first hardware functional unit includes,

a virus information unit to store virus information; and

a virus detection engine to compare each of the instructions to the virus information.

4. (Currently Amended) The processor of claim 3, wherein the virus detection ~~unit~~ engine includes an authentication unit to authenticate a source of the virus information.

5. (Currently Amended) The processor of claim 1, wherein the first hardware functional unit includes a virus information unit, the virus information unit to store a state machine that is to determine whether ones of the instructions are associated with a virus.

6. (Currently Amended) The processor of claim 1, wherein the first hardware functional unit is a virus detection unit and wherein the second hardware functional unit is a dispatch and execution unit.

7. (Currently Amended) A apparatus comprising:

an instruction cache to store instructions;

a hardware virus detection unit within a processor to receive the instructions from the instruction cache, the hardware virus detection unit to determine whether ones of the instructions are associated with a virus; and

a dispatch and execution unit within the processor to receive from the hardware virus detection unit the ones of the instructions that are not associated with the virus.

8. (Currently Amended) The apparatus of claim 7, wherein the hardware virus detection unit includes a virus information unit to store virus signatures, the virus detection unit to compare each of the instructions to the virus signatures.

9. (Currently Amended) The apparatus of claim 8, wherein the hardware virus detection unit includes an authentication unit to authenticate a source of the virus signatures.

10. (Currently Amended) The apparatus of claim 7, wherein the hardware virus detection unit includes a virus information unit to store state information, the hardware virus detection unit to input each of the instructions into a state machine.

11. (Currently Amended) A method comprising:

receiving an instruction in a first functional unit of a processor pipeline, wherein the first functional unit is an integrated circuit within the processor pipeline dedicated to on-chip virus detection;

determining within the first functional unit whether the instruction is associated with a virus; and

after determining the instruction is not associated with a virus, transmitting the instruction to a second functional unit of the processor pipeline for further processing.

12. (Original) The method of claim 11, wherein the determining whether the instruction is associated with a virus includes, comparing the instruction to virus signatures stored in the first functional unit.

13. (Original) The method of claim 11, wherein the determining whether the instruction is associated with a virus includes inputting the instruction into a state machine stored in the first functional unit.

14. (Original) The method of claim 11 wherein the virus is a polymorphic virus.

15. (Original) The method 11, wherein the first functional unit is a virus detection unit, and wherein the second functional unit is a fetch and decode unit.

16. (Original) The method of claim 11, further comprising:
after determining the instruction is associated with a virus, removing the instruction from the processor pipeline.

17. (Original) The method of claim 11, wherein the instruction has been partially processed by a set of one or more functional units of the processor pipeline.

18. (Currently Amended) A processor comprising:

an instruction cache to store instructions;

a virus detection ~~unit~~ circuit to receive the instructions from the instruction cache, the virus detection ~~unit~~ circuit to transmit ones of the instructions that are not associated with a virus, the virus detection ~~unit~~ circuit including,

a virus information unit to store virus signatures and state machine information;

an authentication unit to authenticate the source of the virus signatures and the state machine information; and

a virus detection engine to compare certain of the instructions to the virus signatures, and to input certain of the instructions into a state machine configured according to the state machine information;

a fetch and decode unit to receive ones of the instructions from the virus detection ~~unit~~ circuit; and

a set of one or more execution units to receive ones of the instructions from the fetch and decode unit and to execute the ones of the instructions.

19. (Original) The processor of claim 18, wherein the virus detection engine determines whether ones of the instructions are associated with the virus.

20. (Canceled)

21. (Currently Amended) A system comprising:

a synchronous dynamic random access memory (SDRAM) unit;

a processor coupled to the SDRAM unit, the processor including,

a plurality of functional units including a first functional unit and a second functional unit, the first functional unit to receive instructions, to determine whether ones of the instructions are associated with a virus, and to transmit the ones of the instructions not associated with the virus to the second functional unit; and

wherein the first functional unit is a circuit within the processor dedicated to virus detection.

22. (Original) The system of claim 21, wherein the first functional unit is a virus detection unit, and wherein the second functional unit is a fetch and decode unit.

23. (Original) The system of claim 21, wherein the first functional unit is a virus detection unit and wherein the second functional unit is a dispatch and execution unit.

24. (Original) The system of claim 21, wherein the first functional unit includes,

a virus information unit to store virus information; and

a virus detection engine to compare each of the instructions to the virus information stored in the processor.

25. (Original) The system of claim 21, wherein the virus detection unit includes an authentication unit to authenticate a source of the virus information.

26. (Original) The system of claim 21, wherein the first functional unit includes a virus information unit, the virus information unit to store a state machine for determining whether ones of the instructions are associated with a virus.